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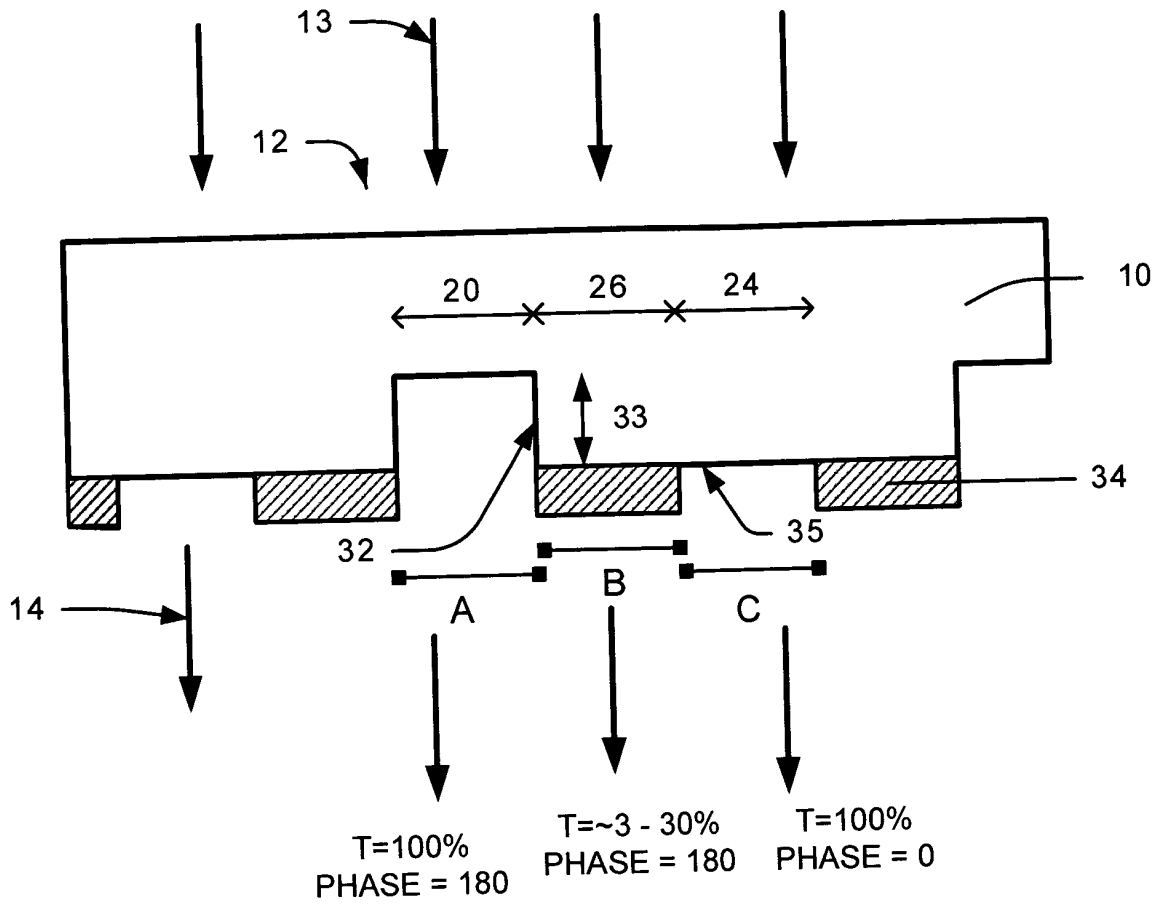


FIGURE 1A

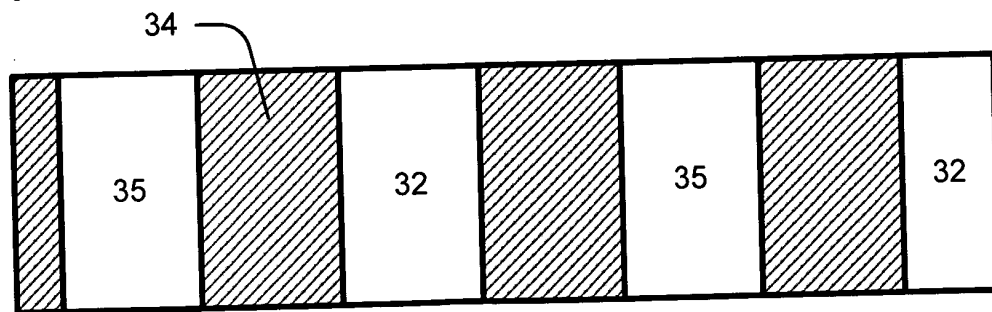


FIGURE 1B

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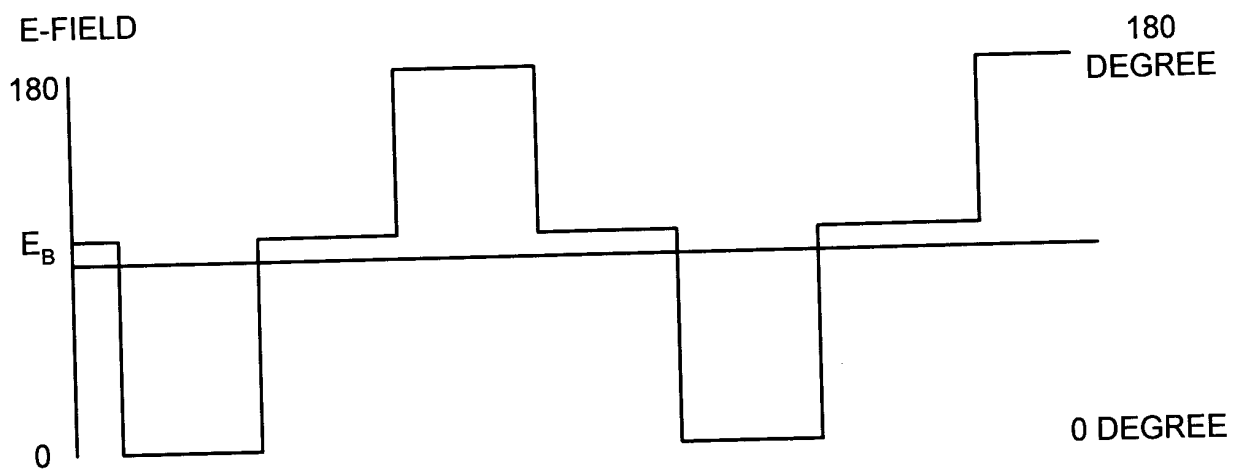
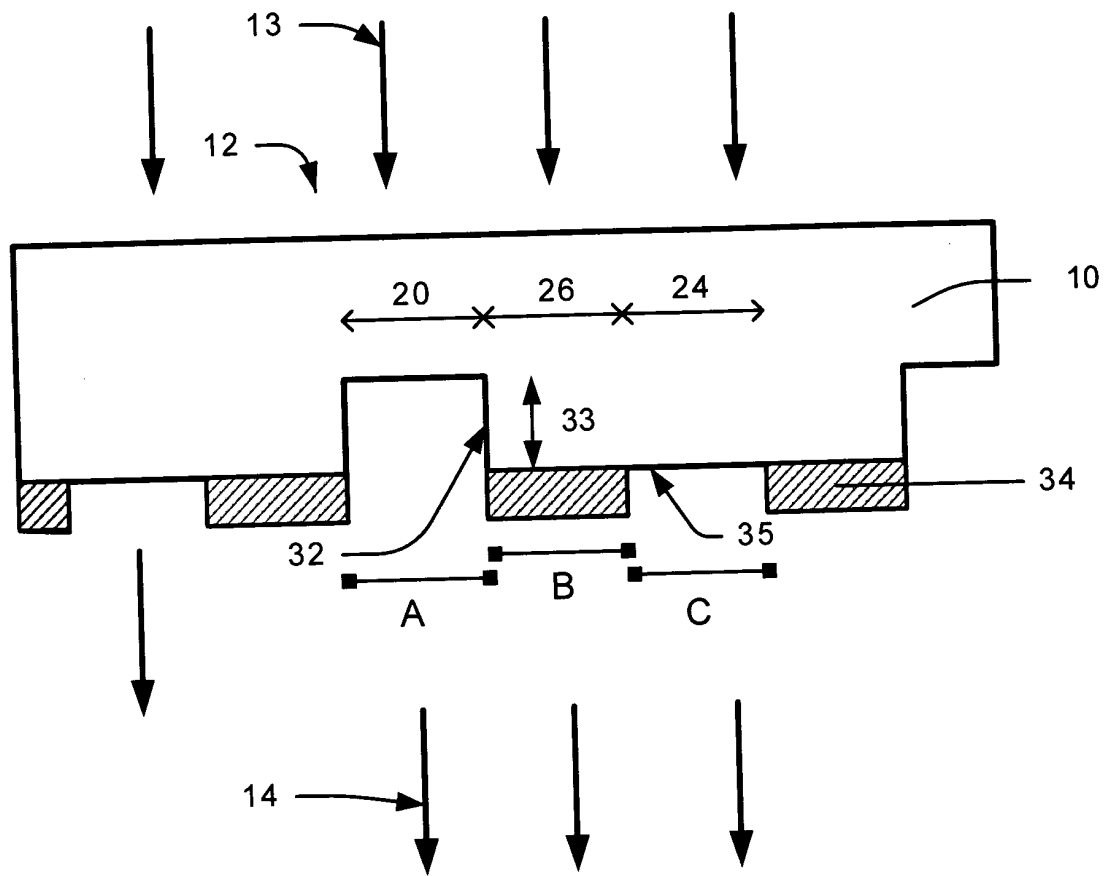


FIGURE 2

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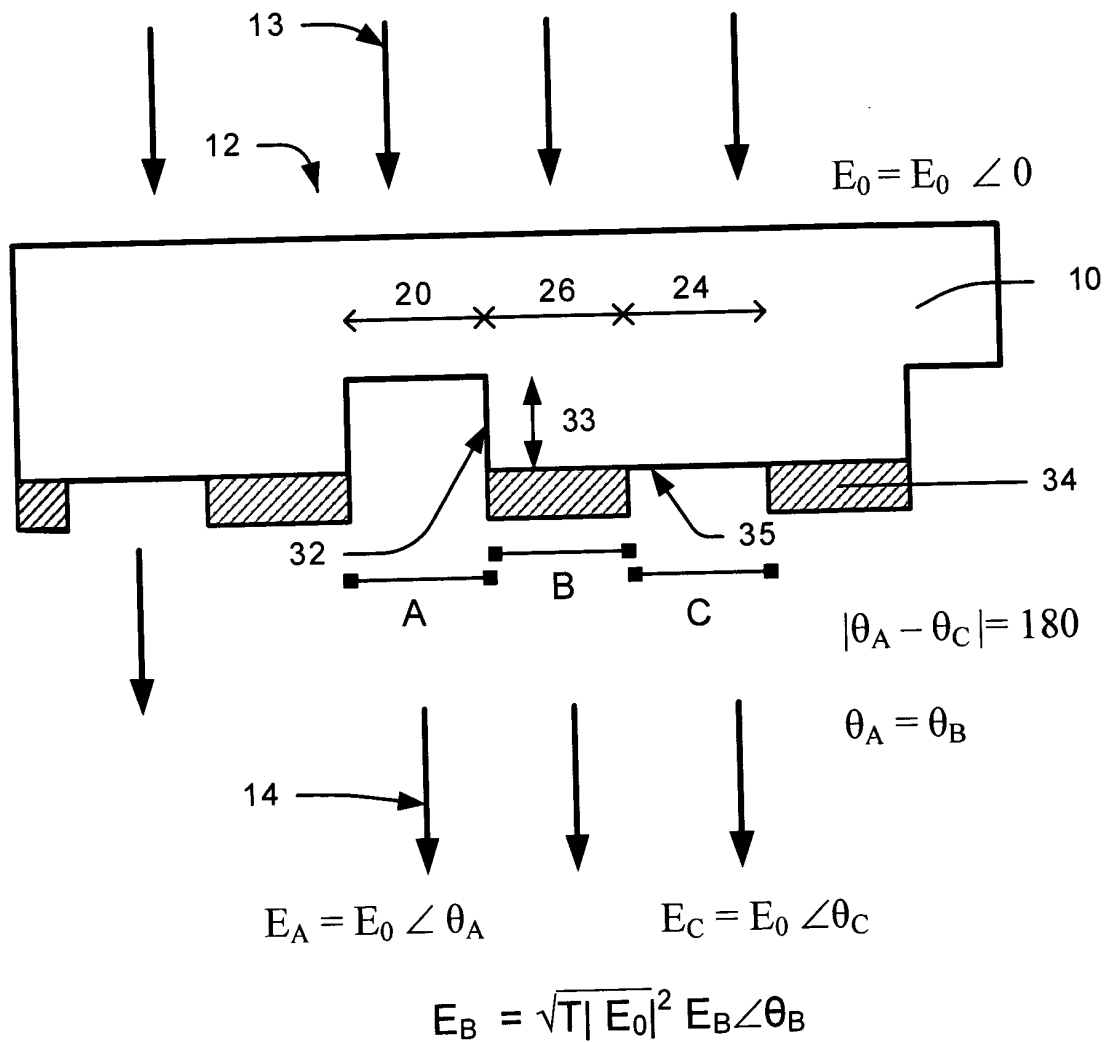


FIGURE 3A

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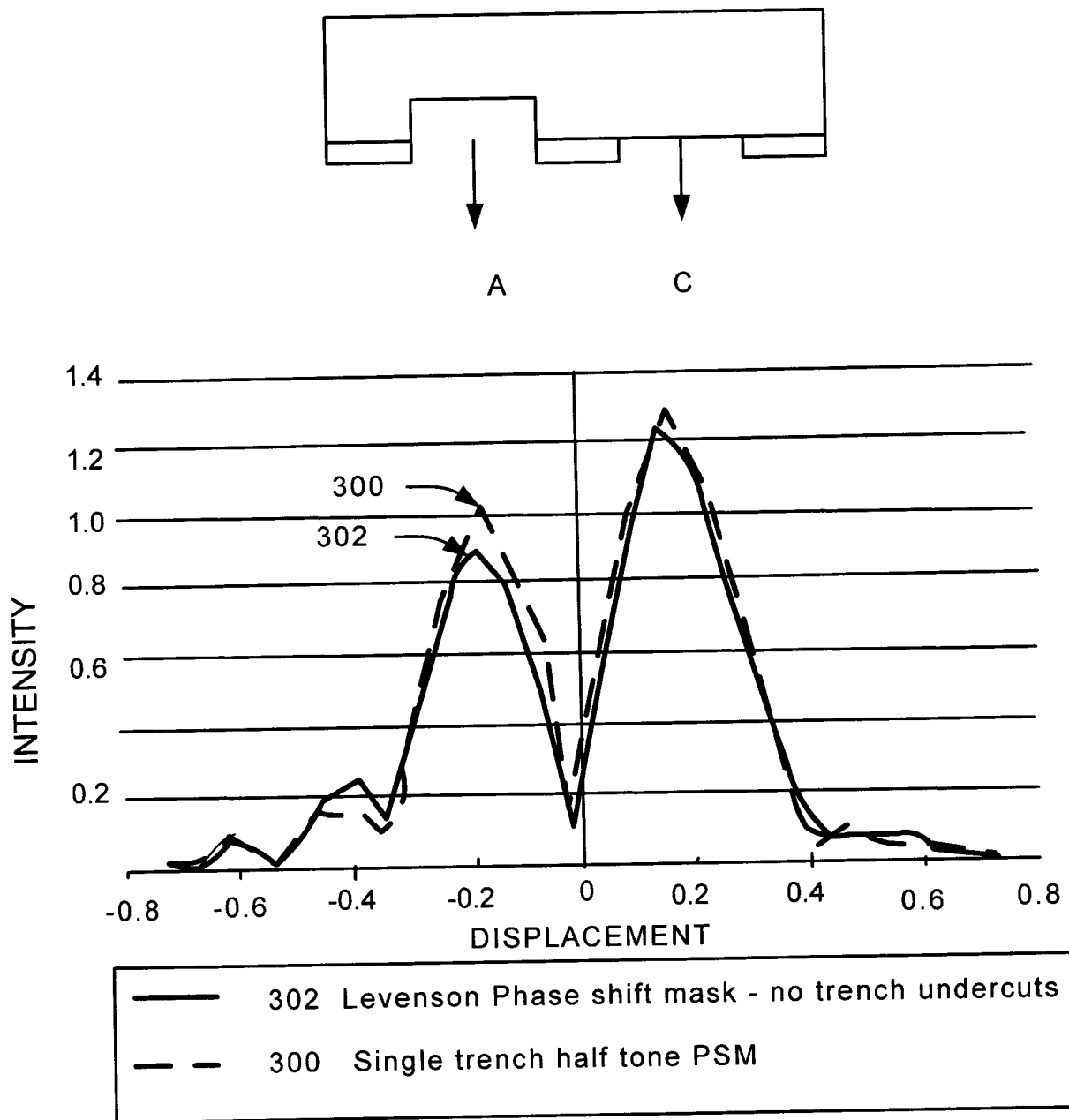


FIGURE 3B

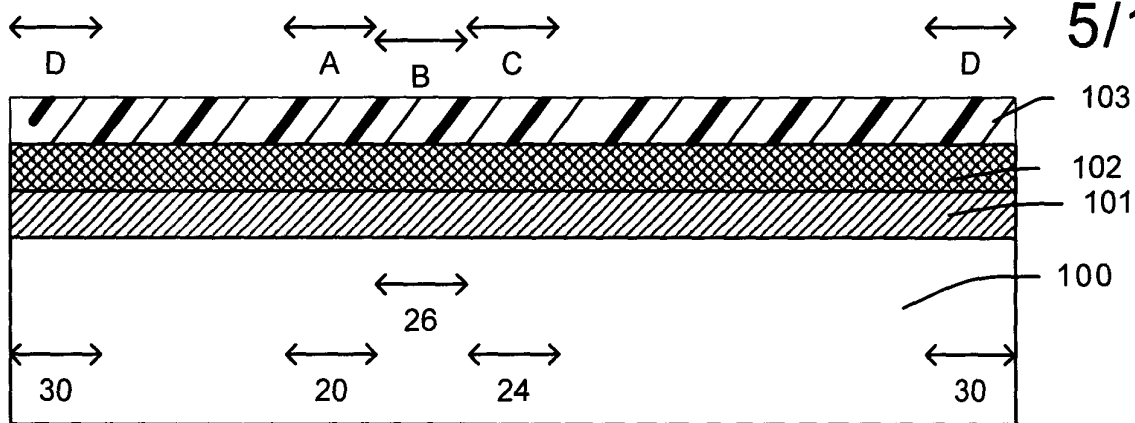


FIGURE 4A

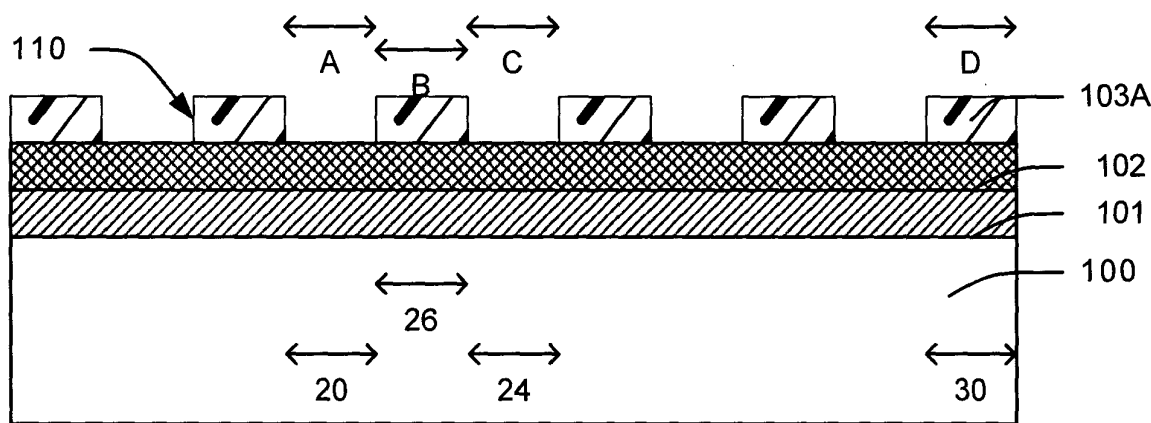


FIGURE 4B

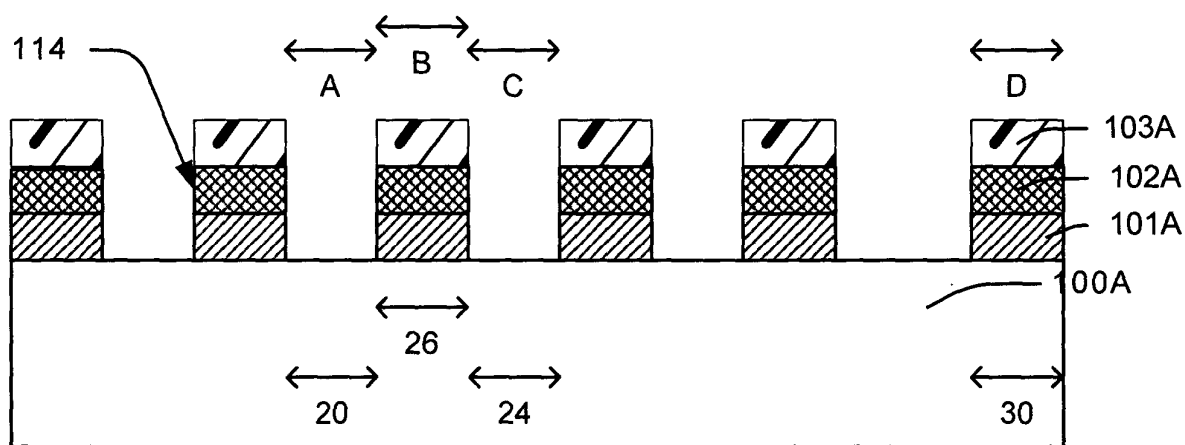


FIGURE 4C

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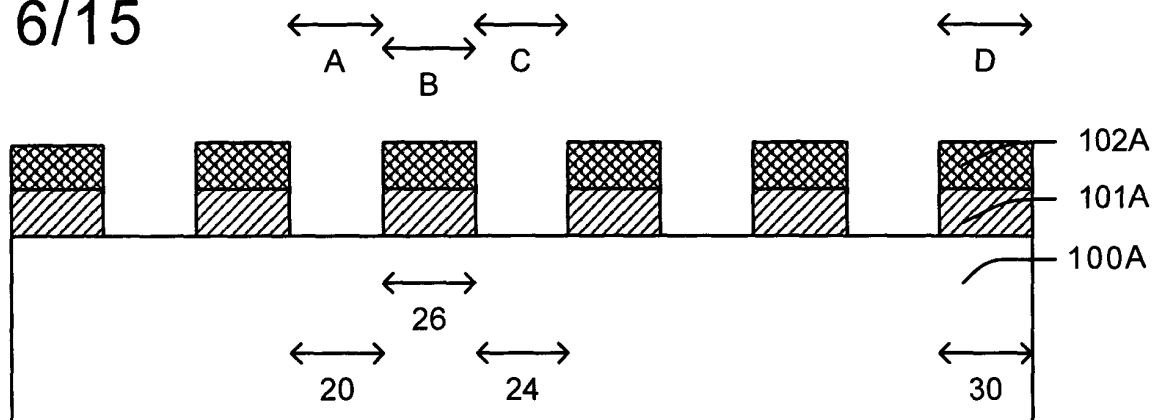


FIGURE 4D

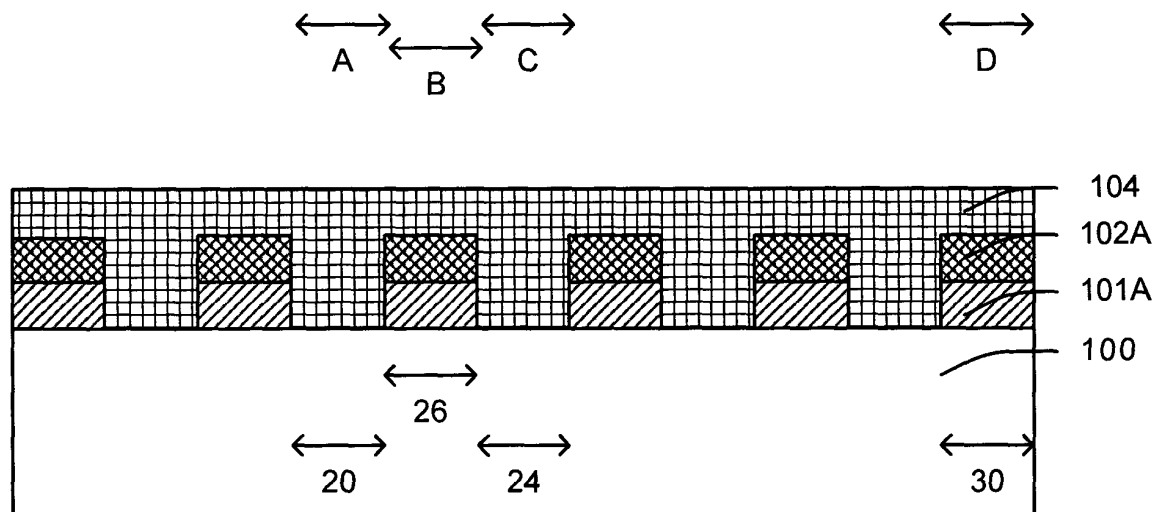


FIGURE 4E

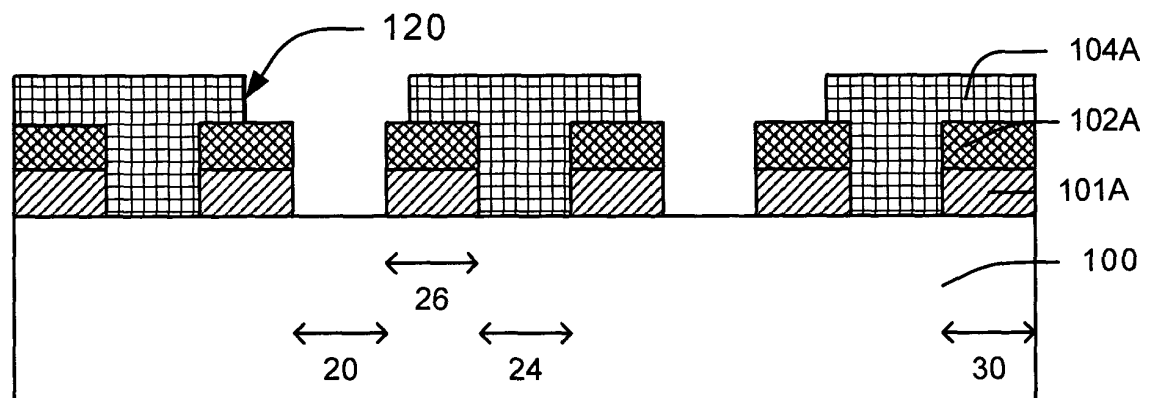


FIGURE 4F

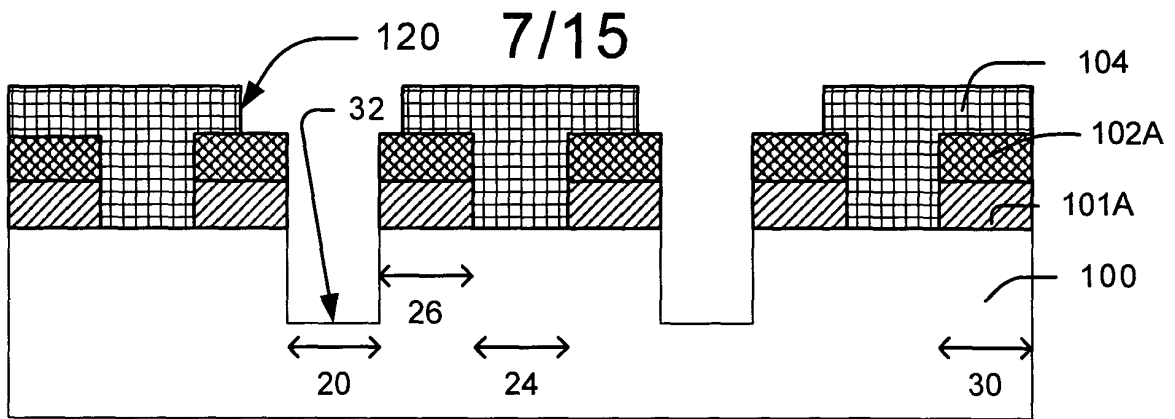


FIGURE 4G

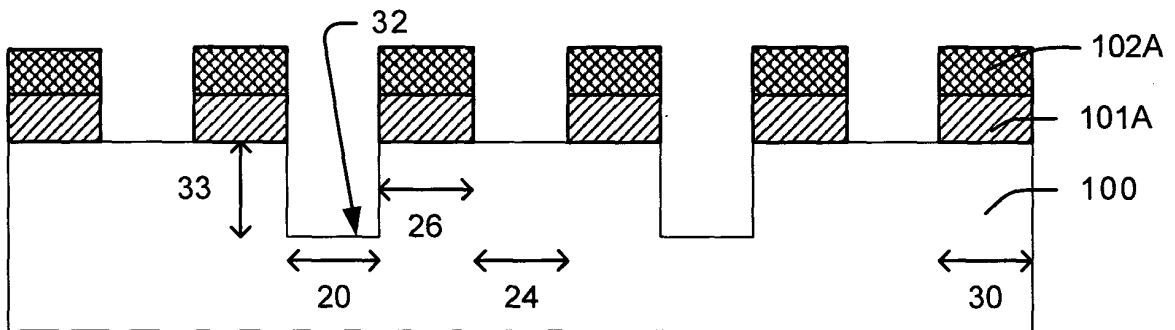


FIGURE 4H

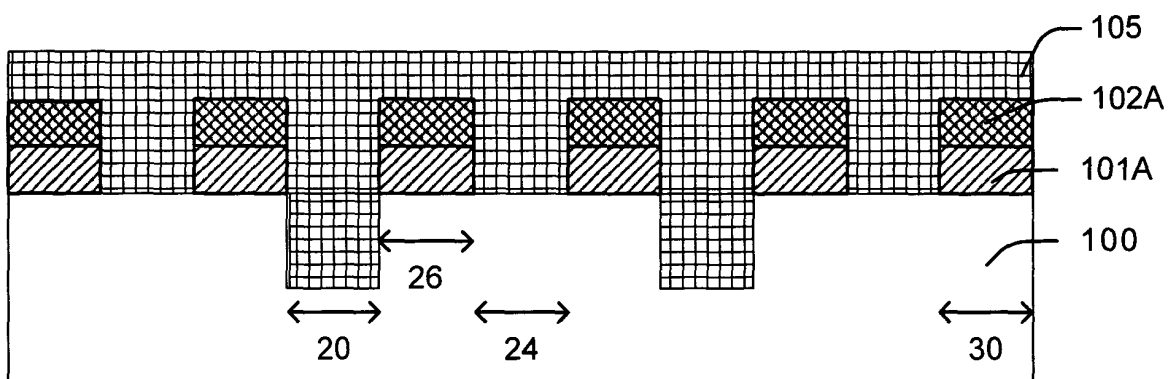


FIGURE 4I

A cross-sectional view of a semiconductor device 100. The device features a series of steps or recesses. The first step has a width of 20 and a depth of 26. The second step has a width of 24. The third step has a width of 30. The final structure 124 is composed of three layers: 101A (bottom, diagonal hatching), 102A (middle, cross-hatching), and 105A (top, grid pattern). A label 32 points to the bottom surface of the first step.

[illegible]

FIGURE 4L



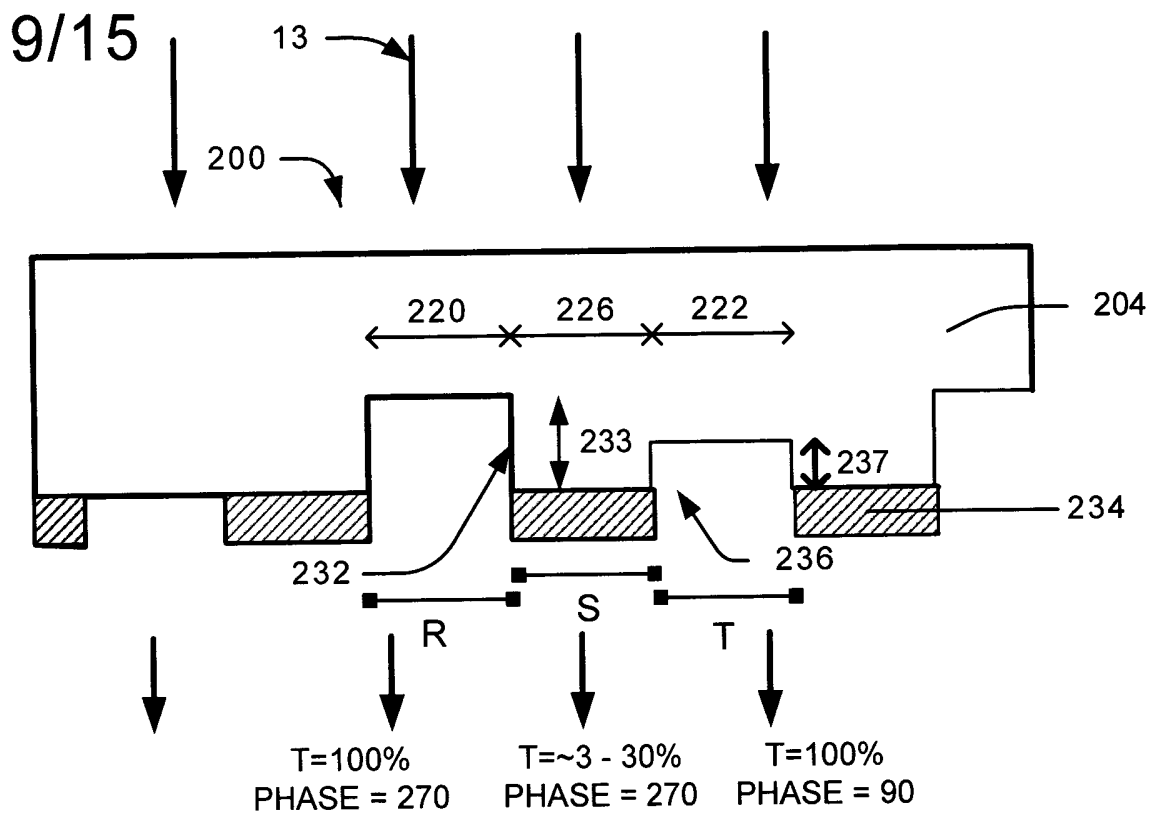


FIGURE 5

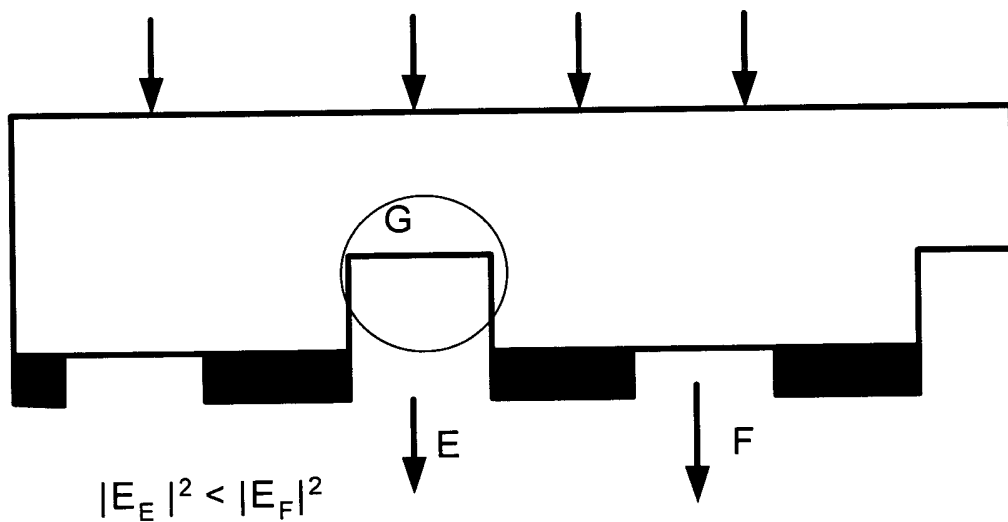


FIGURE 7

--- PRIOR ART

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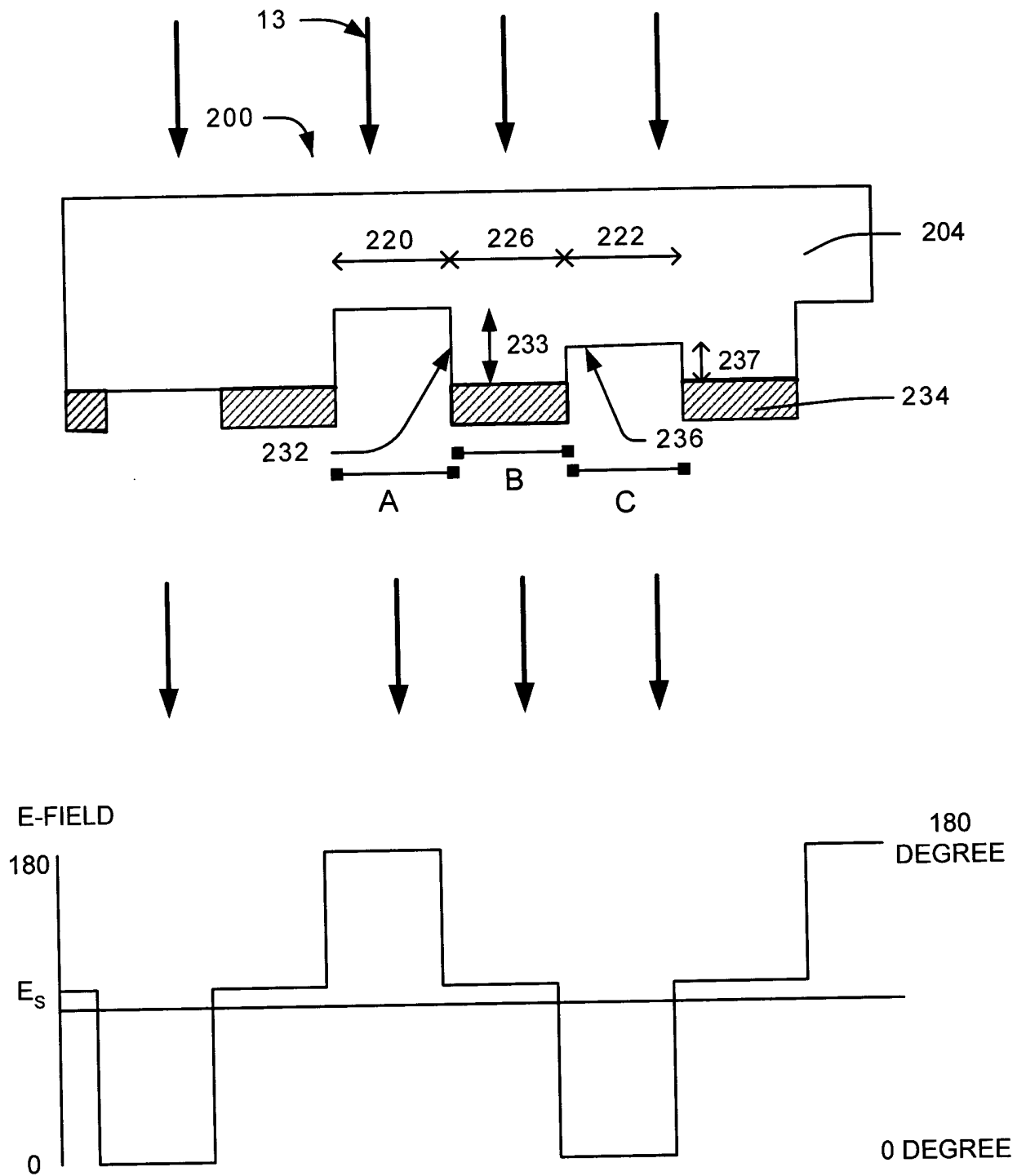


FIGURE 6

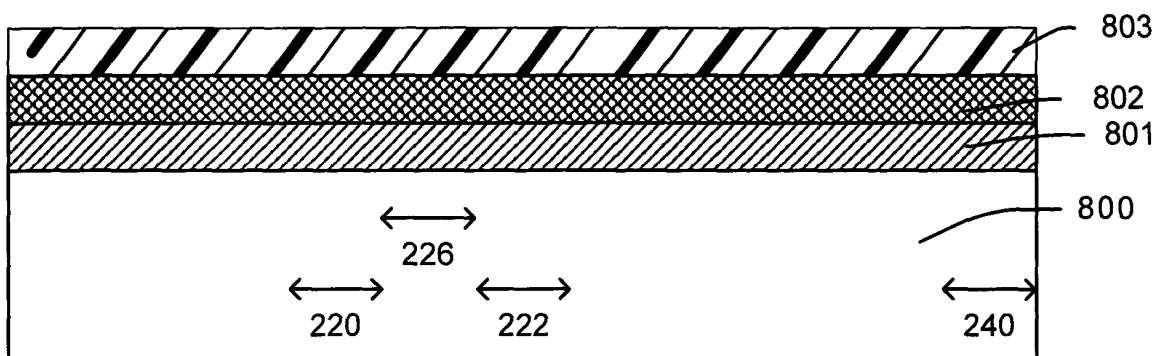


FIGURE 8A

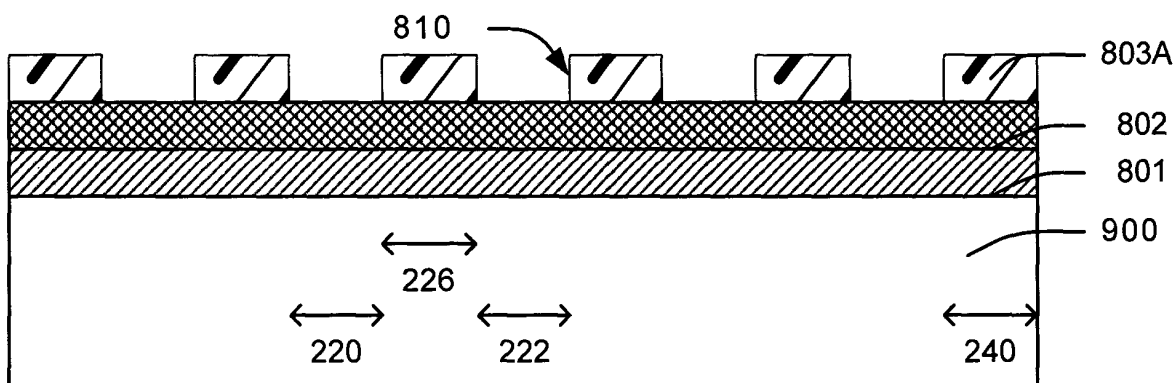


FIGURE 8B

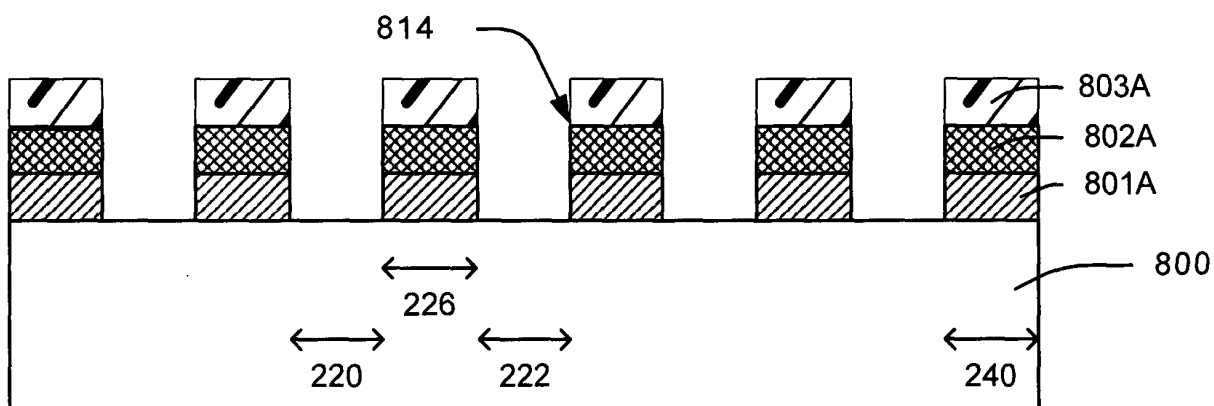


FIGURE 8C

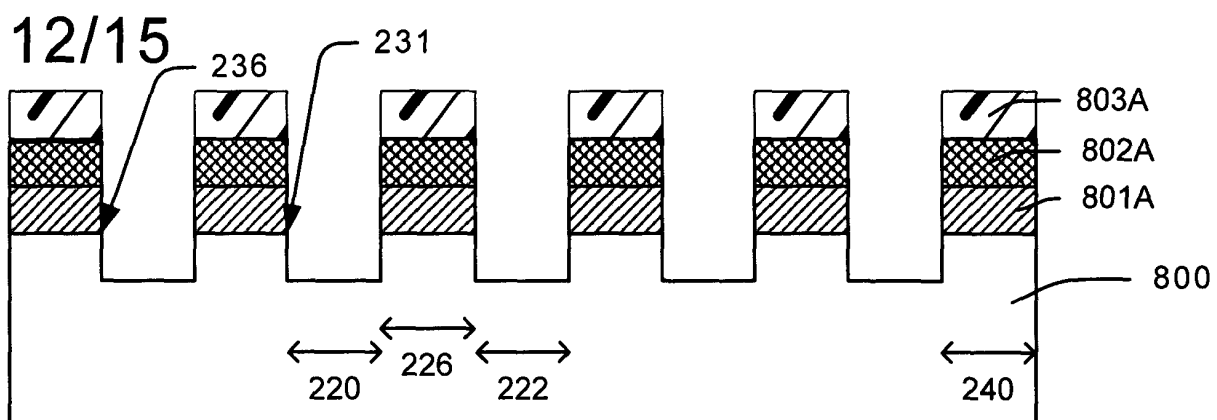


FIGURE 8D

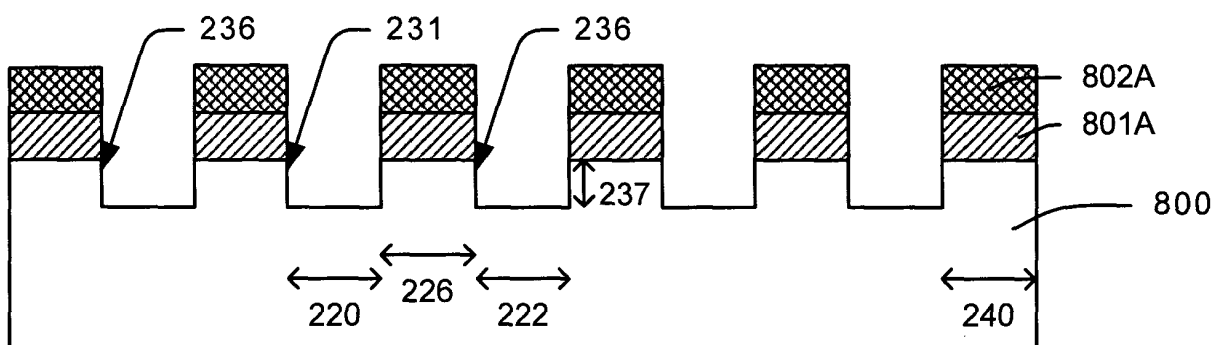


FIGURE 8E

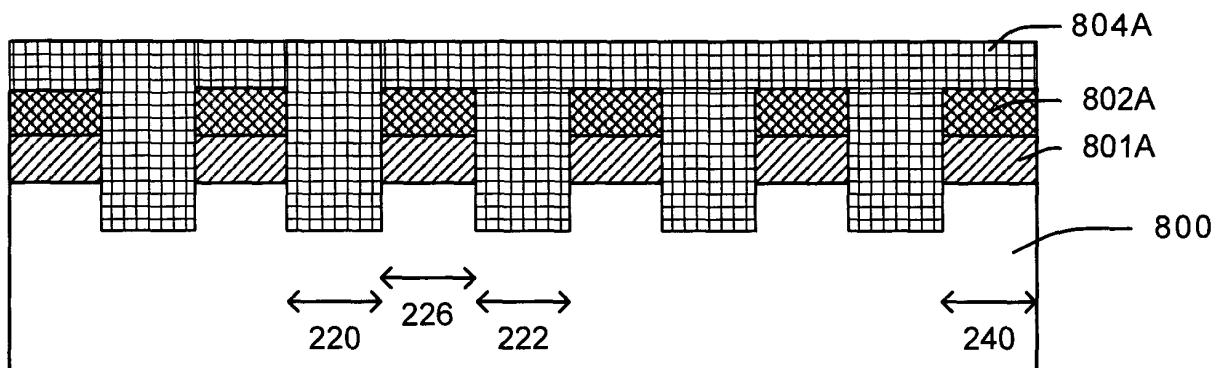


FIGURE 8F

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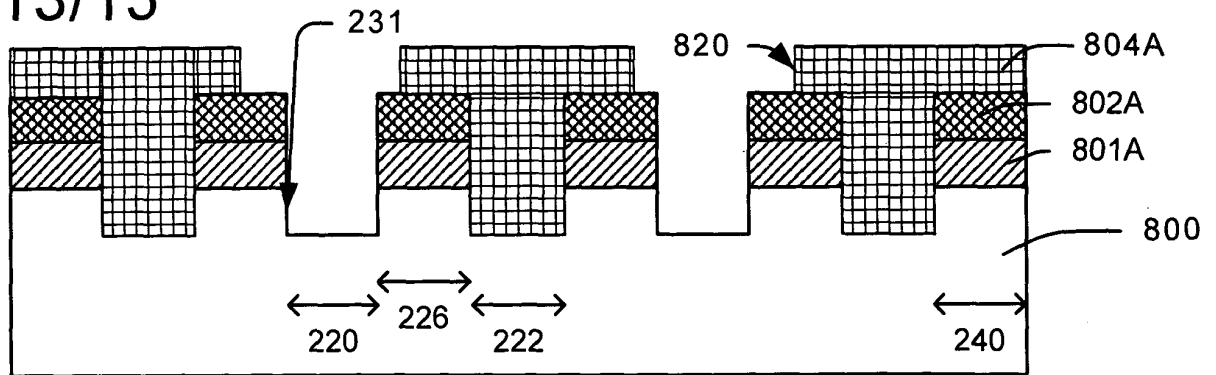


FIGURE 8G

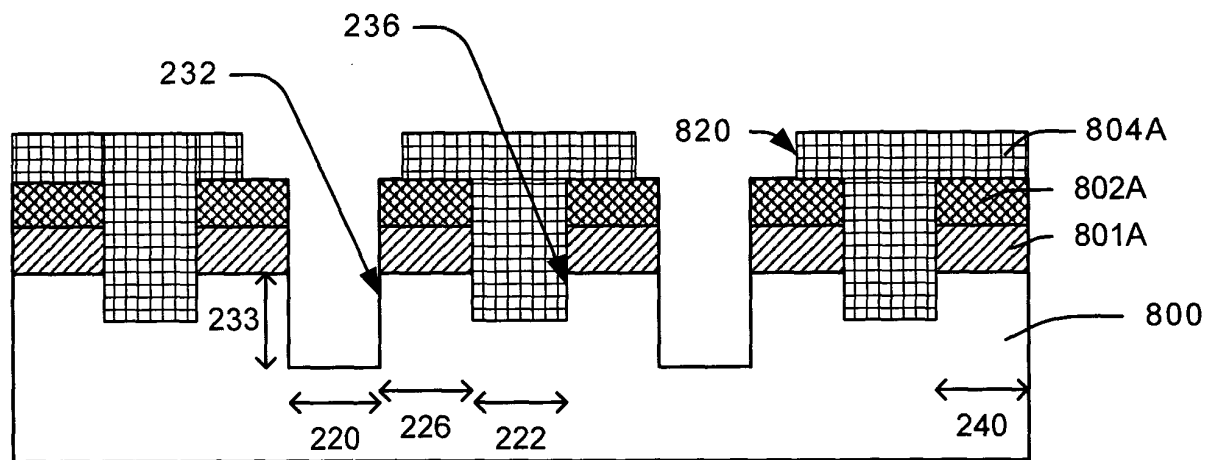


FIGURE 8H

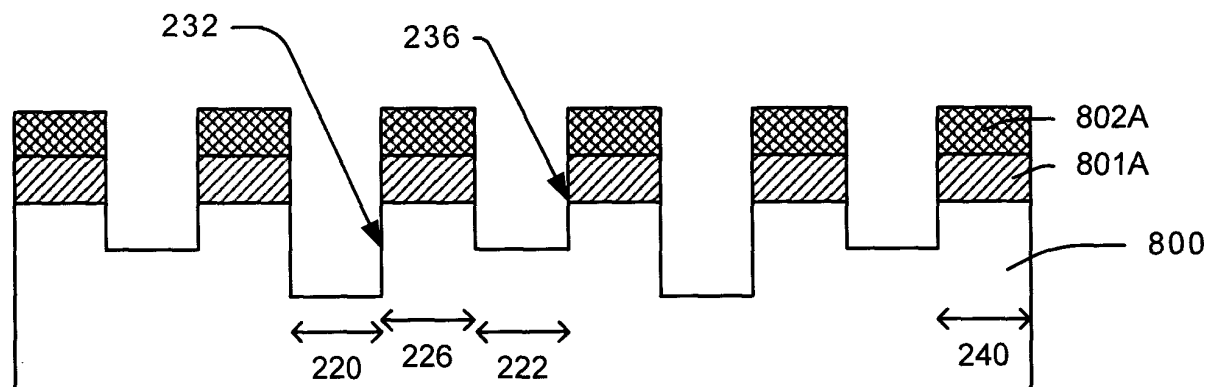


FIGURE 8I

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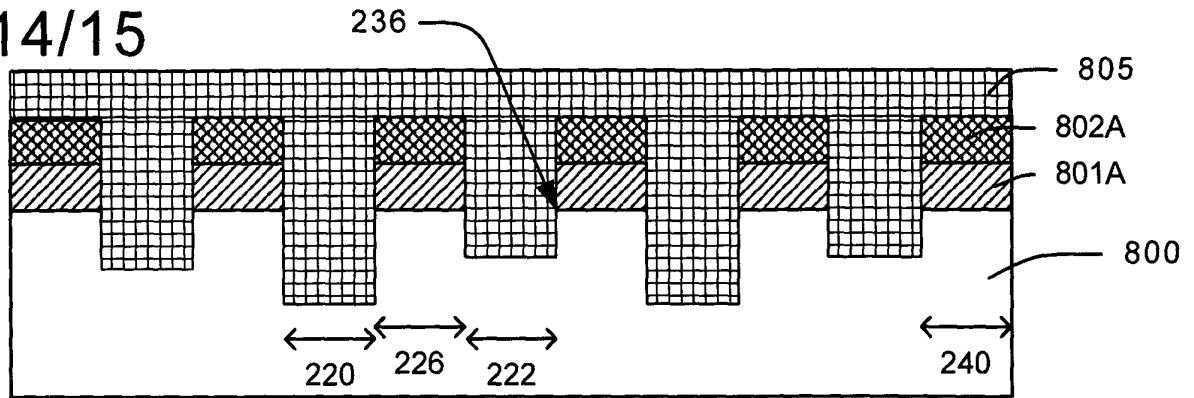


FIGURE 8J

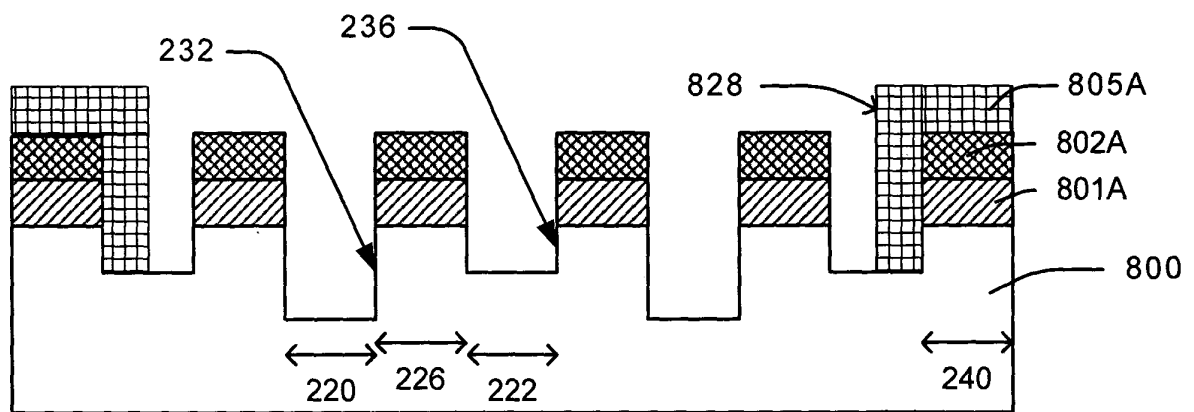


FIGURE 8K

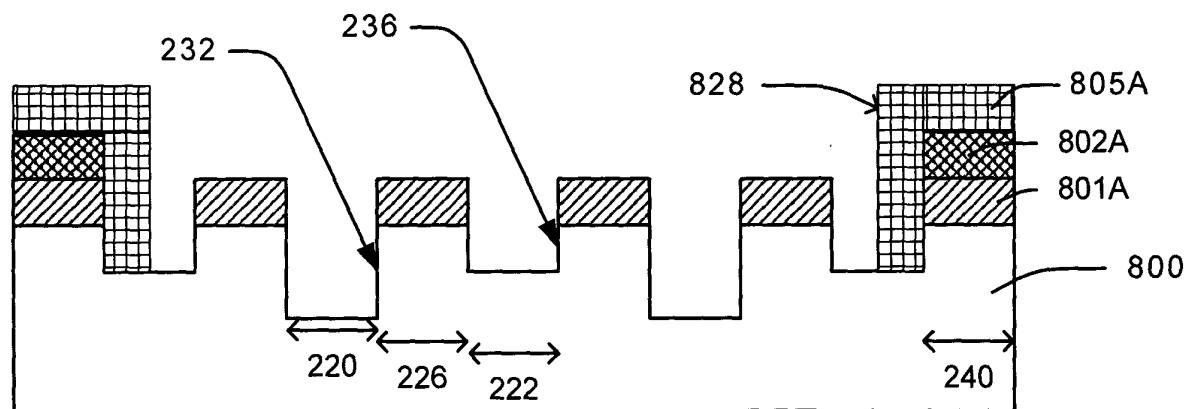


FIGURE 8L

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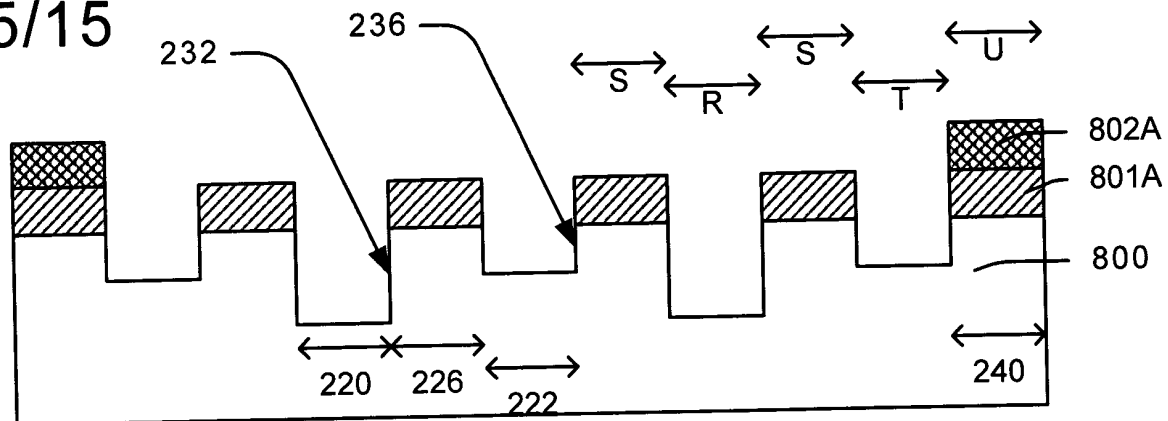


FIGURE 8M

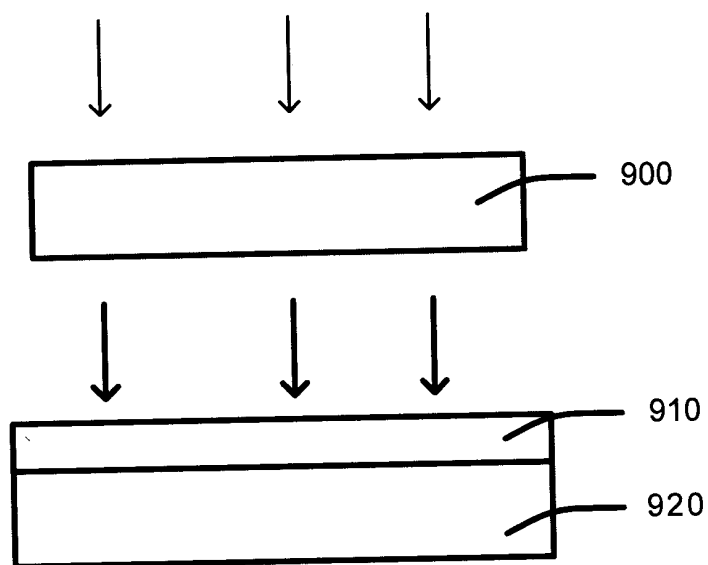


FIGURE 9